PCB Layout and Design Guide for CH7055A Video DAC

1.0 INTRODUCTION

The CH7055A is a device targeting portable and similar systems which accept a digital input signal, and encodes and transmits data through three 10-bit DACs. The device is able to encode the video signals and generate synchronization signals for Analog RGB and composite SYNC signal output.

This application note focuses only on the basic PCB layout and design guidelines for CH7055A Video DAC. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.
The discussion and figures that follow reflect and describe connections based on the 40-pin QFN package of the CH7055A. Please refer to the CH7055A datasheet for the details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7055A should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C2, C3) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7055A ground pins, in addition to ground vias.

2.1.1 Ground Pins

The grounds of the CH7055A is the thermal exposed pad and should be connected to a common ground plane to provide a low impedance return path for the supply currents. Refer to **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

There are three power supply pins, VDDA, VDD18, VDDIO. Refer to **Table 1** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pins Assignment of the CH7055A (QFN)

Pin Assignment	# Of Pins	Type	Symbol	Description
11	1	Power	VDDIO	IO supply voltage (1.8-3.3V)
22	1	Power	VDD18	Digital supply voltage (1.8V)
25	1	Power	VDDA	Analog supply voltage (3.3V)
Thermal pad	1	Ground	GND	Power supply ground

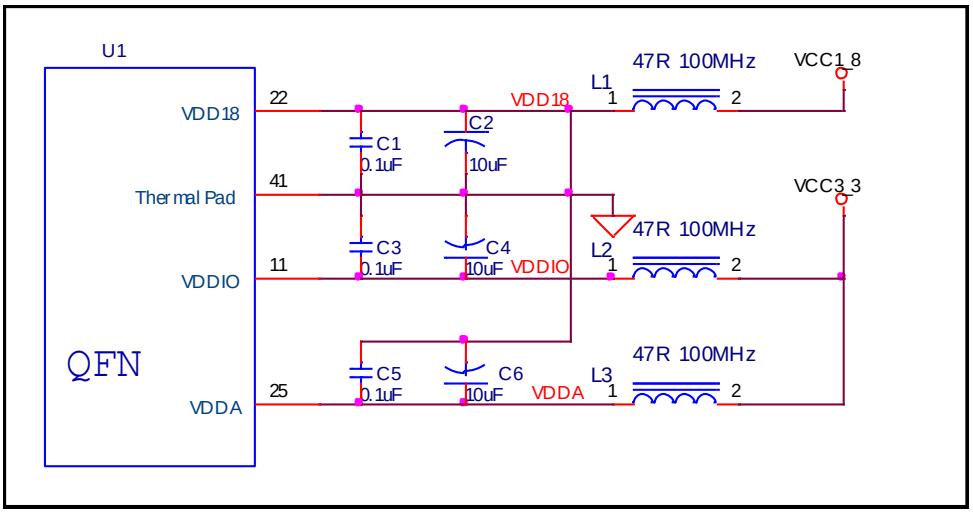
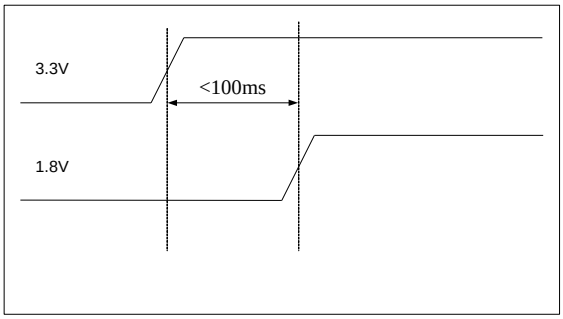


Figure 1: Power Supply Decoupling and Distribution

Note: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05 Ω at DC; 23 Ω at 25MHz & 47 Ω at 100MHz. Please refer to Fair Rite part #2743019447 for details or an equivalent part can be used for the diagram.

• 2.1.3 On chip power-on sequence

The 1.8V must be later than 3.3V and less than 100ms



2.2 Internal Reference Pins

• RSET pin

This pin sets the DAC current. A 1.2 kΩ, 1% tolerance resistor should be connected between RSET and GND as shown in **Figure 2**. A smaller resistance will create more DAC current, resulting brighter TV out images. This resistor should be placed with short and wide traces as near as possible to CH7055A.

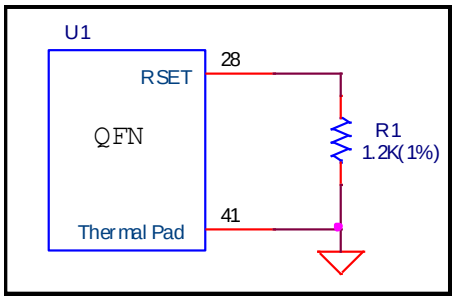


Figure 2: RSET pin connection

2.3 General Control Pins

The CH7055A has a hardware mode that allows using the device without a microcontroller. Hardware mode is selected by connecting the SPPEN pin to ground.

• SPPEN

This pin is pull up internally, and should be pull low to ground directly in the hardware mode. Active High.

• CTYPE

When the SPPEN is pull up, CTYPE can be connect to DE as a input; When the SPPEN is pull low, CTYPE is Csync type select: "0" AND Gate; "1" XOR Gate.

• PSAVE

PSAVE is power save control pin. Reduced power consumption when this pin is pulls low. Better connect to the GPIO pin for the control.

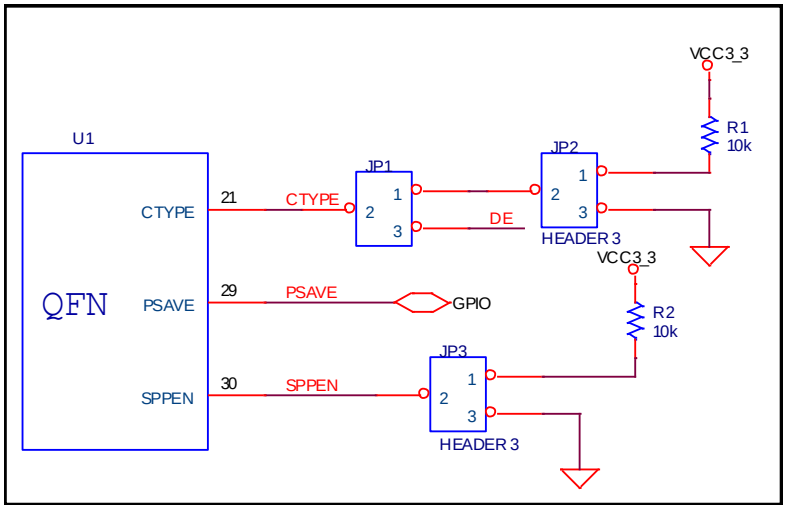


Figure 3: General Control pins

2.4 Serial Port Control for CH7055A

• SC and SD

SD and SC function as a serial interface where SD is bi-directional data and SC is an input only serial clock. In the reference design, SD and SC pins are pulled up to VDDIO (+1.8V ~ +3.3V) with 6.8k Ω resistors always as shown in **Figure 4**.

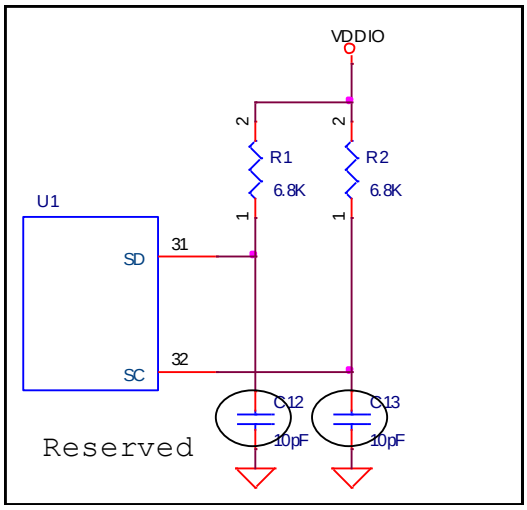


Figure 4: Serial Port Control

2.5 Input Pins

• Data Inputs

CH7055A can accept up to 24 data inputs, as shown in **Figure 5**, from a digital video port of a graphics controller. The swing is defined by VDDIO (1.8 ~ 3.3V).
Unused Data input pins should be pulled low with 10k Ω resistors or shorted to Ground directly.

• H/V Sync Pins

The horizontal/vertical sync pins can be used as inputs as shown in **Figure 5**.

• CTYPE

The CTYPE pin can be used as a data input indicator (Refer to **Figure 5**). When the pin is high, the input data is active. When the pin is low, the input data is blanking.

• CLK

The CLK input is the clock signal input to the device for using with the H, V, DE and D [23:0] data.

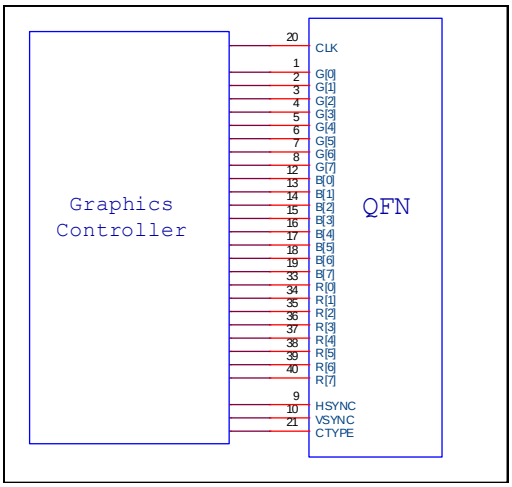


Figure 5: CH7055A Input Pins

2.6 Video Outputs

- **DAC 0~2**

Three on-chip 10-bit high speed DACs provide RGB and csync output. If the DACs require a double termination, A 75 Ω resistor should be placed between each DAC pin and the ground as shown in **Figure 6**.

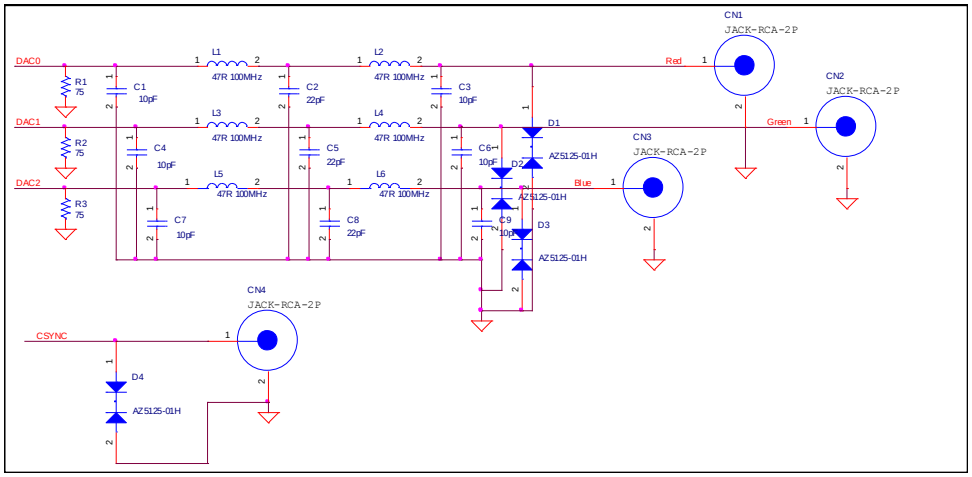
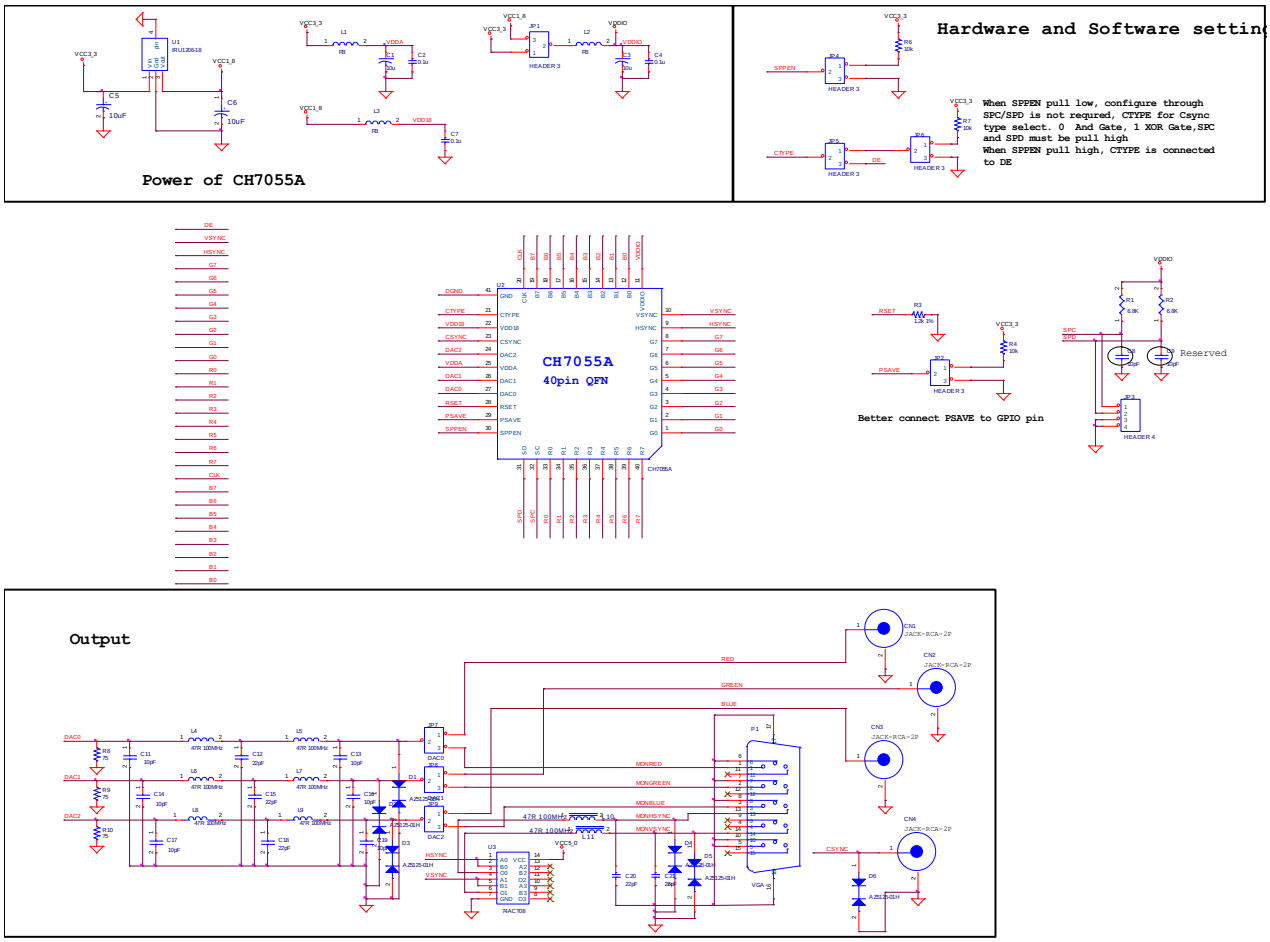


Figure 6: CH7055A Video Output

3.0 REFERENCE DESIGN EXAMPLE

The figures below are the reference schematic of CH7055A, which is provided here for design reference only. Please contact Chrontel Applications group for further support. **Table 2** provides the BOM list for the reference schematic.

3.1 Reference Schematic



3.2 Reference Board Preliminary BOM

Table 2: CH7055A Reference Design BOM List

Item	Quantity	Reference	Part
1	4	CN1, CN2, CN3, CN4	RCA Jack
2	4	C1, C3, C5, C6	10 μF
3	3	C2, C4, C7	0.1 μF
4	8	C8, C9, C11, C13, C14, C16, C17, C19	10 pF
5	5	C12, C15, C18, C20, C21	22 pF
6	6	D1, D2, D3, D4, D5, D6	AZ5125-01H
7	8	JP1, JP2, JP4, JP5, JP6, JP7, J8, JP9	Header 3
8	1	JP3	Header 4
9	3	L1, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11	47R 100MHz
10	1	P1	VGA
11	2	R1, R2	6.8K
12	1	R3	1.2K 1%
13	3	R4, R6, R7	10K
14	3	R8, R9, R10	75
15	1	U1	IRU1206-18
16	1	U2	CH7055A
17	1	U3	74ACT08

4.0 REVISION HISTORY

Table 3: Revisions

Rev. #	Date	Section	Description
1.0	05/02/2012	All	Initial release
1.1	06/28/2018	2.1	Add Power-on sequence
1.2	06/30/2020	Disclaimer	Update the disclaimer

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